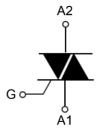
$I_{T(RMS)}$ = 8 A

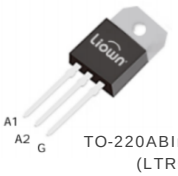
V_{DRM}/V_{RRM} = 800 V

I_{GT} (1) = 10 to 25 mA

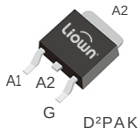
LTR08A,LTR08B,LTR08D, LTR08I,LTR08D²

8A Snubberless™, logic level and standard Triacs

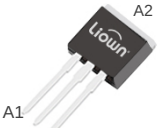




TO-220ABInsulated (LTR08)



D²PAK(LTR08D)



IPAK(LTR08I)

Features

- On-state rms current, IT(RMS) 8 A
- Repetitive peak off-state voltage, VDRM / VRRM 800 V
- Triggering gate current, IGT 10 to 25 mA

Description

Available either in through-hole and surface-mount packages, these devices are suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits or for phase control operation in light dimmers and motor speed controllers, etc.

The Snubberless versions are specially recommended for use on inductive loads, thanks to their high commutation performance

Logic level versions are designed to interface directly with low power drivers such as Microcontrollers.

Absolute maximum ratings (T_j = 25 °C unless otherwise stated)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	IPAK, DPAK,TO-220AB, D²PAK	T_c = 110 °C	8	A
		TO-220AB Ins.	T_c = 100 °C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25 °C)	f = 50 Hz	t = 20 ms	80	A
		f = 60 Hz	t_p = 16.7 ms	84	
I^2t	I^2t value for fusing		t_p = 10 ms	36	A^2s
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT}, tr ≤ 100 ns	f = 120 Hz	T =j125 °C	50	A/µs
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 125 °C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125 °C	1	W
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +125	°C

Electrical characteristics (T_j = 25 °C, unless otherwise specified) - Snubberless and logic level (3 quadrants)

Symbol	Parameter	Quadrant		LTR08			LTR08A / LTR08B				Unit
				10	35	50	TW	SW	CW	BW	
I_{GT} (1)	V_D = 12 V, R_L = 30 Ω	I - II - III	Max.	10	35	50	5	10	35	50	mA
V_{GT}		I - II - III	Max.	1.2							V
V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ, T_j = 125 °C	I - II - III	Min.	0.2							V
I_H (2)	I_T = 100 mA	I - II - III	Max.	15	35	75	10	15	35	50	mA
I_L	I_G = 1.2 x I_{GT}	I - III	Max.	25	50	70	10	25	50	70	mA
		II	Max.	30	60	110	15	30	60	80	
dV/dt (2)	V_D = 67% V_{DRM}, gate open, T_j = 125 °C		Max.	40	400	1000	20	40	400	1000	V/µs
(dI/dt)c (2)	(dV/dt)c = 0.1 V/µs, T_j = 125 °C		Min.	5.4			3.5	5.4			A/ms
	(dV/dt)c = 10 V/µs, T_j = 125 °C		Min.	2.8			1.5	2.98			
	Without snubber, T_j = 125 °C		Min.		4.5	7			4.5	7	

Standard (4 quadrants)

Symbol	Parameter	Quadrant		LTR08A / LTR08B		Unit
				C	B	
I_{GT} (1)	V_D = 12 V, R_L = 33 Ω	I - II - III	Max.	25	50	mA
		IV		50	100	
V_{GT}		All	Max.	1.3		V
V_{GD}	V_D = V_{DRM}, R_L = 33 kΩ, T_j = 125 °C	All	Min.	0.2		V
I_H (2)	I_T = 500 mA	I - II - III	Max.	25	50	mA
I_L	I_G = 1.2 I_{GT}	I - III - IV	Max.	40	50	mA
		II		80	100	
dV/dt (2)	V_D = 67 % V_{DRM} gate open, T_j = 125 °C		Min.	200	400	V/µs
(dV/dt)c (2)	(dI/dt)c = 3.5 A/ms, T_j = 125 °C		Min.	5	10	V/µs

Static electrical characteristics

Symbol	Test conditions			Value	Unit
V_{TM} (1)	I_{TM} = 11 A, t_p = 380 µs	T_j = 25 °C	Max.	1.35	V
V_{TO} (1)	threshold on-state voltage	T_j = 125 °C	Max.	0.85	V
R_D (1)	Dynamic resistance	T_j = 125 °C	Max.	50	mΩ
I_{DRM} I_{RRM}	V_{DRM} = V_{RRM}	T_j = 25 °C	Max.	5	µA
		T_j = 125 °C	Max.	1	mA

Thermal resistance

Symbol	Parameter			Value	Unit
$R_{th(j-c)}$	Max. junction to case thermal resistance (AC)		IPAK / D2PAK / DPAK / TO-220AB	1.6	°C/W
			TO-220AB Insulated	2.5	
$R_{th(j-a)}$	Junction to ambient (typ.)	S = 2 cm² (1)	D²PAK	45	°C/W
		S = 1 cm²(1)	DPAK	70	
	Junction to ambient (typ.)		TO-220AB / TO-220AB Insulated	60	
			IPAK	100	

Figure 1. Maximum power dissipation versus on-state RMS current (full cycle)

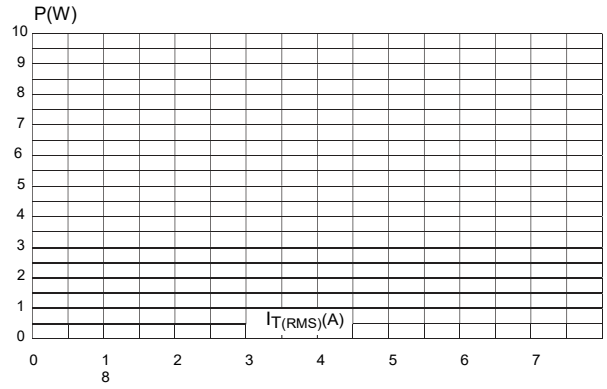


Figure 2. RMS on-state current versus temperature (full cycle)

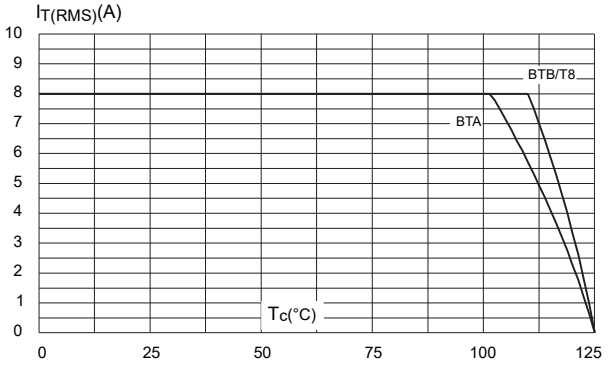


Figure 3. RMS on-state current versus ambient temperature (full cycle)

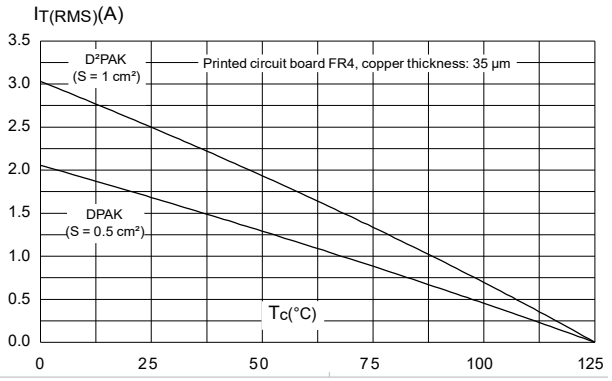


Figure 4. Relative variation of thermal impedance versus pulse duration

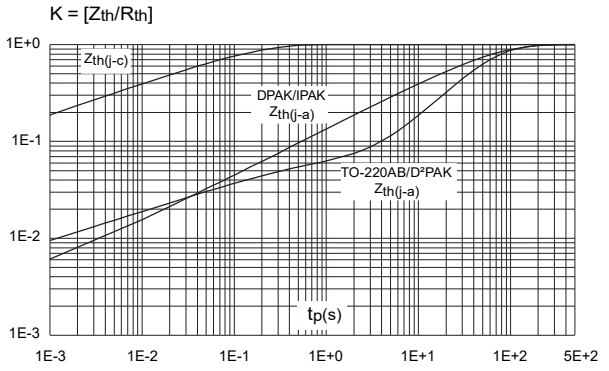


Figure 5. On-state characteristics (maximum values)

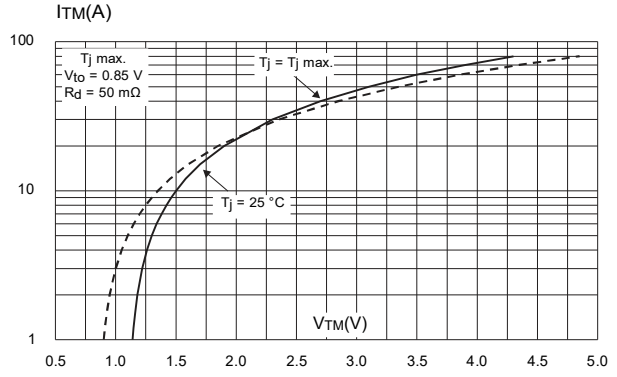


Figure 6. Surge peak on-state current versus number of cycles

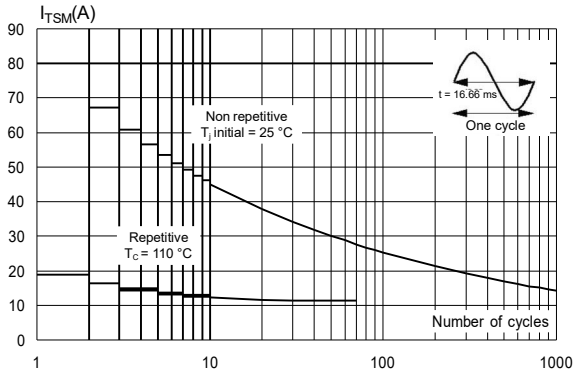


Figure 7. Non repetitive surge peak on-state current for a sinusoidal pulse (t_p < 10 ms)

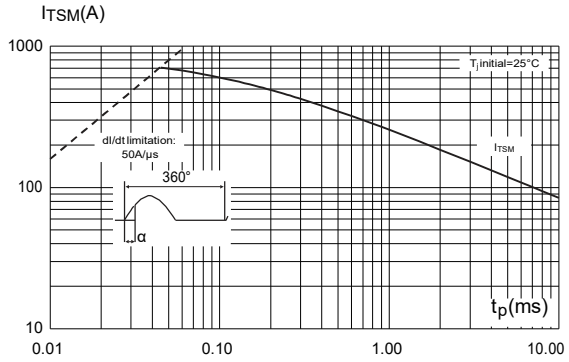


Figure 8. Relative variation of gate trigger current

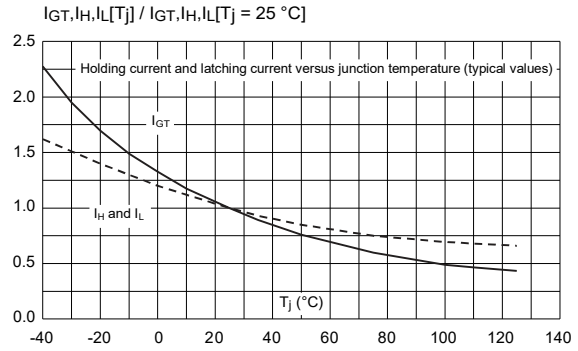


Figure 9. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

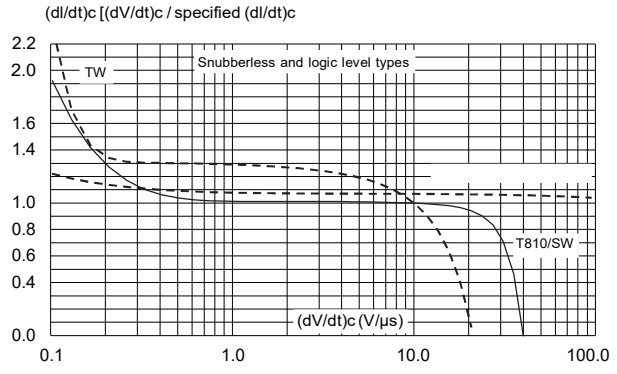


Figure 10. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

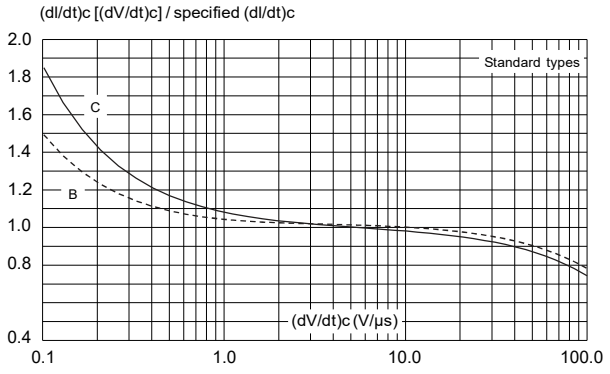


Figure 11. Relative variation of critical rate of decrease of main current versus junction temperature

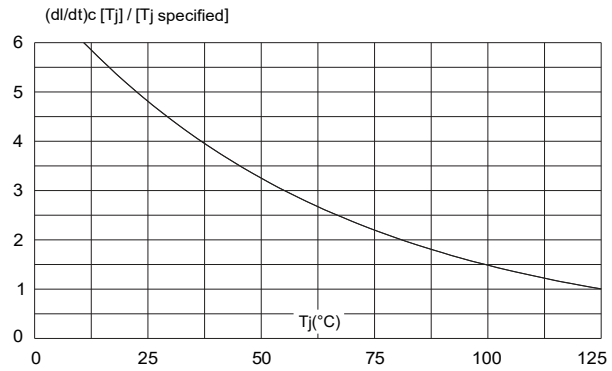


Figure 12. DPAK and D2PAK thermal resistance junction to ambient versus copper surface under tab