LTR16A,LTR16B,LTR16D
16A Snubberless™, logic level and standard Triacs

$I_{T(RMS)}$ = 16 A
V_{DRM}/V_{RRM} = 800 V
I_{GT} **(Snubberless)** = 10 to 25 mA
IGT (Standard) = 25 to 70 mA

Features

- Medium current Triac
- Low thermal resistance with clip bonding
- Low thermal resistance insulation ceramic for insulated LTR
- High commutation (4Q) or very high commutation (3Q) capability

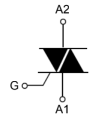
Description

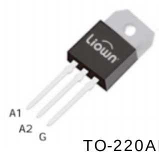
Available either in through-hole or surface mount packages, the LTR16 Triac series are suitable for general purpose mains power AC switching. They can be used as ON/OFF function in applications such as static relays, heating regulation or induction motor starting circuit.They are also recommended for phase control operations in light dimmers and appliance motors speed controllers

The Snubberless™ versions are especially recommended for use on inductive loads, because of their high commutation performance.

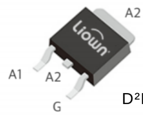
Applications

- LTR16 versions especially recommended for use on inductive loads, because of their high commutation performances
- On/off or phase angle function in applications such as static relays, light dimmers and appliance motor speed controllers





TO-220AB
(LTR16)



D²PAK(LTR16D)

Absolute maximum ratings

Symbol	Parameters			Value	Unit
IT(RMS)	RMS on-state current (full sine wave)	TO-220AB, D2PAK	Tc = 100 °C	16	A
		TO-220AB Ins.	Tc = 86 °C		
ITSM	Non repetitive surge peak on-state current (full cycle, Tj initial = 25 °C)	F = 50 Hz	tp = 20 ms	160	A
		F = 60 Hz	tp = 16.7 ms	168	
I2t	I2t value for fusing	tp = 10 ms		144	A2s
dI/dt	Critical rate of rise of on-state current IG = 2 x IGT , tr ≤ 100 ns	F = 120 Hz	Tj = 125 °C	50	A/µs
VDSM/VRSM	Non repetitive surge peak off-state voltage	tp = 10 ms	Tj = 25 °C	VDRM/VRRM + 100	V
IGM	Peak gate current	tp = 20 µs	Tj = 125 °C	4	A
PG(AV)	Average gate power dissipation		Tj = 125 °C	1	W
Tstg	Storage junction temperature range			-40 to +150	°C
Tj	Operating junction temperature range			-40 to +125	°C

Static electrical characteristics

Symbol	Test conditions	T_j		Value	Unit
V_T (1)	I_{TM} = 22.5 A, t_p = 380 µs	25 °C	Max.	1.35	V
V_{TO} (1)	threshold on-state voltage	125 °C	Max.	0.85	V
R_D (1)	Dynamic resistance	125 °C	Max.	25	mΩ
I_{DRM}/I_{RRM}	$V_{DRM} = V_{RRM}$	25 °C	Max.	5	µA
		125 °C		2	mA

For both polarities of A2 referenced to A1

Electrical characteristics (T_j = 25 °C, unless otherwise specified) - standard (4 quadrants)

Symbol	Parameters	Quadrant		LTR16A LTR16B		Unit
				C	B	
I_{GT} (1)	V_D = 12 V, R_L = 33 Ω	I - II - III	Max.	25	50	mA
		IV		50	100	
V_{GT}		All	Max.	1.3		V
V_{GD}	$V_D = V_{DRM}$, R_L = 3.3 kΩ, T_j = 125 °C	All	Min.	0.2		V
I_H (2)	I_T = 500 mA		Max.	25	50	mA
I_L	I_G = 1.2 I_{GT}	I - III - IV	Max.	40	60	mA
		II	Max.	80	120	

Symbol	Parameters	Quadrant		LTR16A LTR16B		Unit
				C	B	
dV/dt(2)	V_D = 67 % V_{DRM} gate open, T_j = 125 °C		Min.	200	400	V/µs
(dV/dt)c(2)	(dI/dt)c = 7 A/ms, T_j = 125 °C		Min.	5	10	V/µs

1. Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.
2. For both polarities of A2 referenced to A1

Electrical characteristics (T_j = 25 °C, unless otherwise specified) - (3 quadrants)

Symbol	Parameters	Quadrant		LTR1610 / LTR16A- SW LTR16B- SW	LTR1635 / LTR16A-CW LTR16B-CW	LTR1650 / LTR16A-BW LTR16B-BW	Unit
I_{GT}(1)	V_D = 12 V, R_L = 30 Ω	I - II - III	Max.	10	35	50	mA
V_{GT}			Max.	1.3			V
V_{GD}	V_D = V_{DRM}, R_L = 3,3 kΩ, T_j = 125 °C		Min.	0.2			V
I_H(2)	I_T = 500 mA		Max.	15	35	50	mA
I_L	I_G = 1.2 I_{GT}	I - III	Max.	25	50	70	mA
		II	Max.	30	60	80	
(dV/dt)(2)	VD = 67 % V_{DRM} gate open, T_j = 125 °C		Min.	40	500	1000	V/µs
(dI/dt)c(2)	(dV/dt)c = 0.1 V/µs, T_j = 125 °C		Min.	8.5			A/ms
	(dV/dt)c = 10 V/µs, T_j = 125 °C			3.0			
	Without snubber, T_j = 125 °C				8.5	14	

1. Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.
2. For both polarities of A2 referenced to A1

Thermal resistance

Symbol	Parameters		Value	Unit
$R_{th(j-c)}$	Max. junction to case (AC)	TO-220AB / D²PAK	1.2	°C/W
		TO-220AB insulated	2.1	
$R_{th(j-a)}$	Junction to ambient (S = 2 cm²)	D²PAK	45	
	Junction to ambient	TO-220AB / TO-220AB ins	60	

1. Copper surface under tab.

Figure 2. Maximum power dissipation versus on-state RMS current (full cycle)

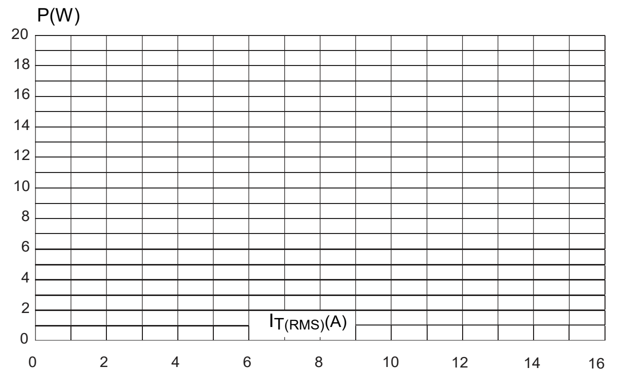


Figure 3. RMS on-state current versus case temperature (full cycle)

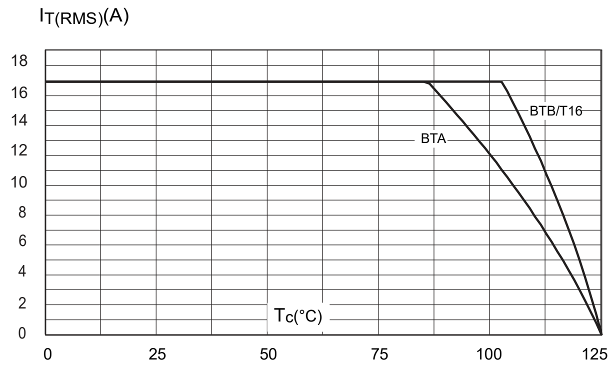


Figure 4. On-state rms current versus ambient temperature (full cycle)

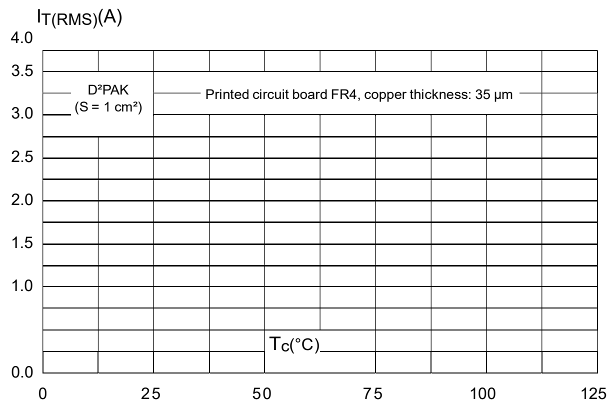


Figure 5. Relative variation of thermal impedance versus pulse duration

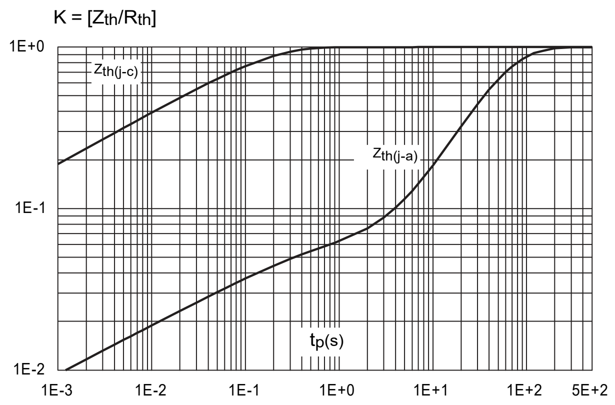


Figure 6. On-state characteristics (maximum values)

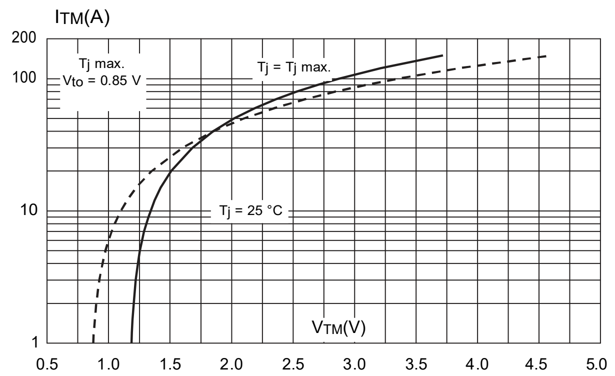


Figure 7. Surge peak on-state current versus number of cycles

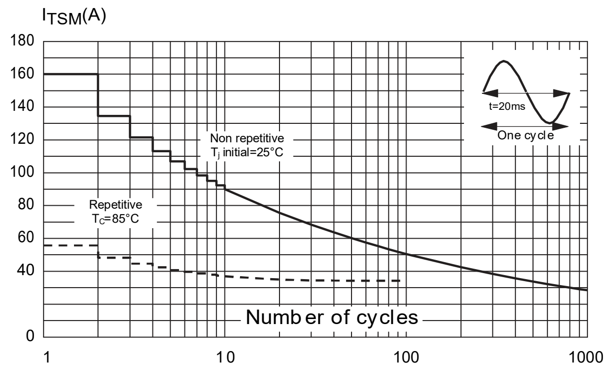


Figure 8. Non-repetitive surge peak on-state current for a sinusoidal

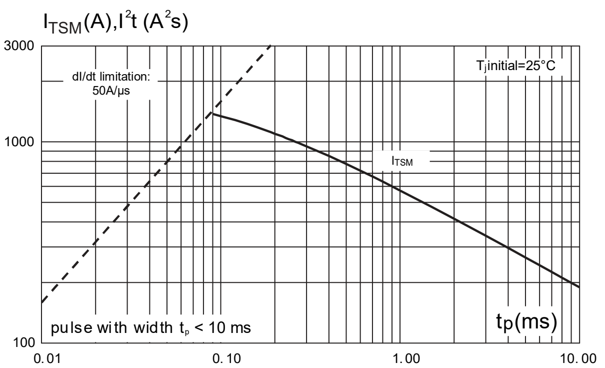


Figure 9. Relative variation of gate trigger current

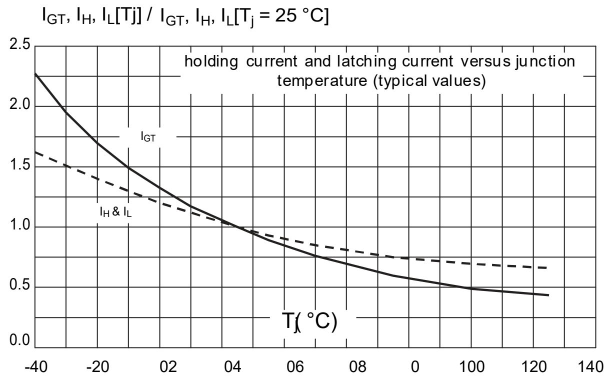


Figure 10. Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values)

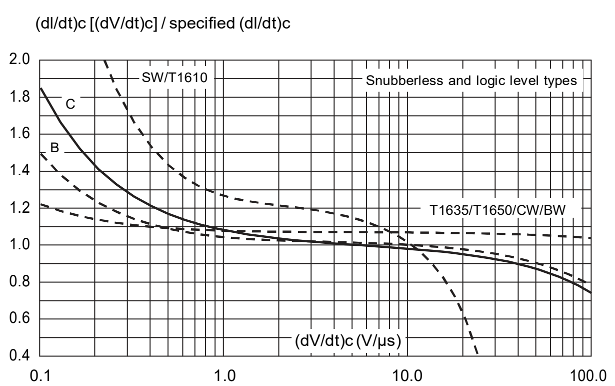


Figure 11. Relative variation of critical rate of decrease of main current versus (junction temperature (typical values)