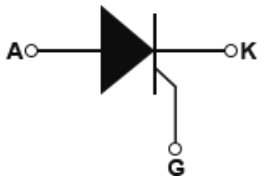
$I_{T(AV)}$	5 A
V_{DRM}/V_{RRM}	800 V
I_{GT}	200 μA
T_J	-40°C to +110°C

LCRW50
Sensitive 8A SCRs

Features

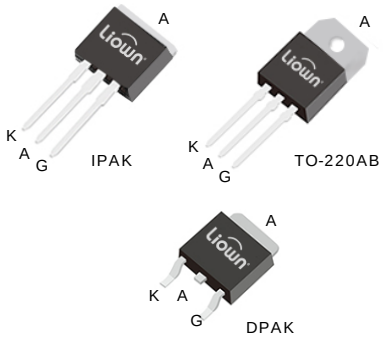
- On-state rms current, $I_{T(RMS)}$ 8A
- Repetitive peak off-state voltage, V_{DRM}/V_{RRM} 800V
- Triggering gate current, I_{GT} 200μA



Description

Available in sensitive LCRW50 gate triggering levels, the 8A SCR series is suitable to fit all modes of control found in applications such as overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, inrush current limiting circuits, capacitive discharge ignition and voltage regulation circuits.

Available in through-hole or surface-mount packages, they provide an optimized performance in a limited space.



Absolute ratings (limiting values)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	On-state rms current (180° conduction angle)		T_c = 110 °C T0-220FPAB, T_c = 91 °C	8	A
$I_{T(AV)}$	Average on-state current (180° conduction angle)		T_c = 110 °C T0-220FPAB, T_c = 91 °C	5	A
I_{TSM}	Non repetitive surge peak on-state	t_p = 8.3 ms t_p = 10 ms	T_j = 25 °C	60 70	A
I^2t	I^2t value for fusing	t_p = 10 ms	T_j = 25 °C	24.5	A^2S
dI/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100$ ns	F = 60 Hz	T_j = 125 °C	50	A/μs
I_{GM}	Peak gate current	t_p = 20 μs	T_j = 125 °C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 125 °C	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 -40 to +110	°C
V_{RGM}	Maximum peak reverse gate voltage			5	V

Sensitive electrical characteristics (T_j = 25 °C, unless otherwise specified)

Symbol	Test conditions			LCRW50	Unit
I_{GT}	V_D = 12 V, R_L = 140 Ω		MAX.	200	µA
V_{GT}			MAX.	0.8	V
V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ, R_{GK} = 220 Ω	T_j = 125 °C	MIN.	0.1	V
V_{RG}	I_{RG} = 10 µA		MIN.	8	V
I_H	I_T = 50 mA, R_{GK} = 1 kΩ		MAX.	5	mA
I_L	I_G = 1 mA ,, R_{GK} = 1 kΩ		MAX.	6	mA
dV/dt	V_D = 65% V_{DRM}, R_{GK} = 220 Ω	T_j = 125 °C	MIN.	5	V/µs
V_{TM}	I_{TM} = 16 A, t_p = 380 µs	T_j = 25 °C	MAX.	1.35	V
V_{t0}	Threshold voltage	T_j = 125 °C	MAX.	0.85	V
R_d	Dynamic resistance	T_j = 125 °C	MAX.	46	mΩ
I_{DRM} I_{RRM}	V_{DRM} = V_{RRM}, R_{GK} = 220 Ω	T_j = 25 °C	MAX.	5	µA
		T_j = 125 °C		1	mA

Standard electrical characteristics (T_j = 25 °C, unless otherwise specified)

Symbol	Test conditions						Unit
I_{GT}	V_D = 12 V, R_L = 33 Ω		MIN.		0.5		mA
			MAX.		5		
V_{GT}			MAX.		1.3		V
V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ	T_j = 125 °C	MIN.		0.2		V
I_H	I_T = 100 mA , gate open		MAX.	25	40	30	mA
I_L	I_G = 1.2 I_{GT}		MAX.	30	50	70	mA
dV/dt	V_D = 67% V_{DRM}, gate open	T_j =125 °C	MIN.	50	150	150	V/µs
V_{TM}	I_{TM} = 16 A t_p = 380 µs	T_j = 25 °C	MAX.		1.35		V
V_{t0}	Threshold voltage	T_j = 125 °C	MAX.		0.85		V
R_d	Dynamic resistance	T_j = 125 °C	MAX.		46		mΩ
I_{DRM} I_{RRM}	V_{DRM} = V_{RRM}	T_j = 25 °C	MAX.		5		µA
		T_j = 125 °C			2		mA

Thermal resistance

Symbol	Parameter			Value	Unit
$R_{th(j-c)}$	Junction to case (DC)		DPAK, IPAK, TO-220AB	1.3	°C/W
			TO-220FPAB	4.6	
$R_{th(j-a)}$		$S^{(1)}$ = 0.5 cm^2	DPAK	70	°C/W
	Junction to ambient (DC)		IPAK	100	
			TO-220AB, TO-220FPAB	60	

1. S = Copper surface under tab

Figure 1. Maximum average power dissipation versus average on-state current

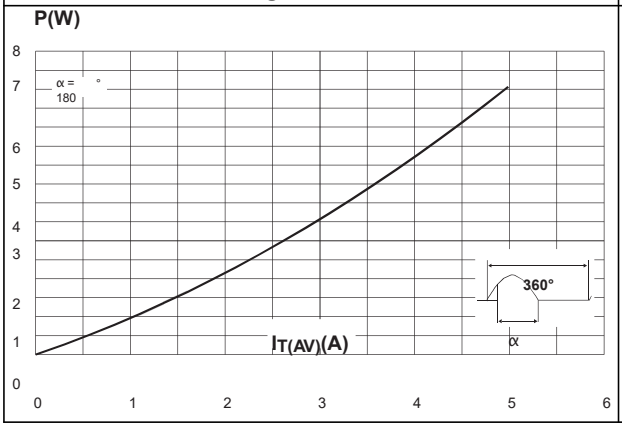


Figure 2. Average and DC on-state curr ent versus case temperature

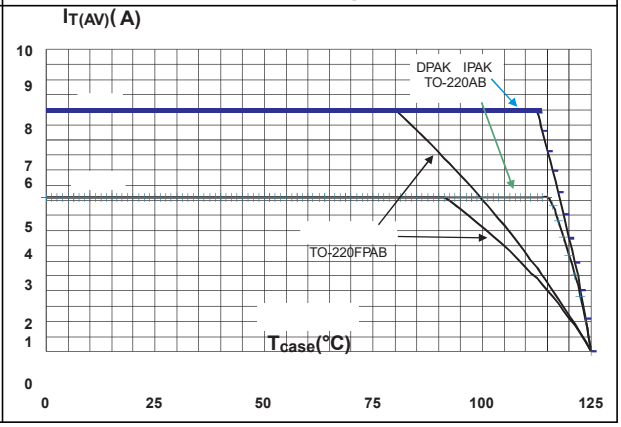


Figure 3. Average and DC on-state current versus ambient temperature

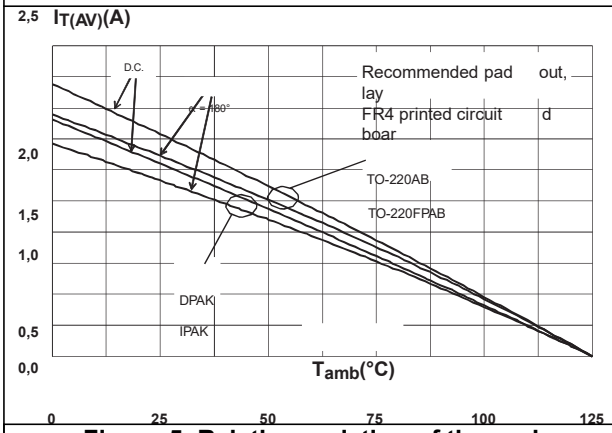


Figure 4. Relative variation of thermal impedance junction to case versus pulse duration

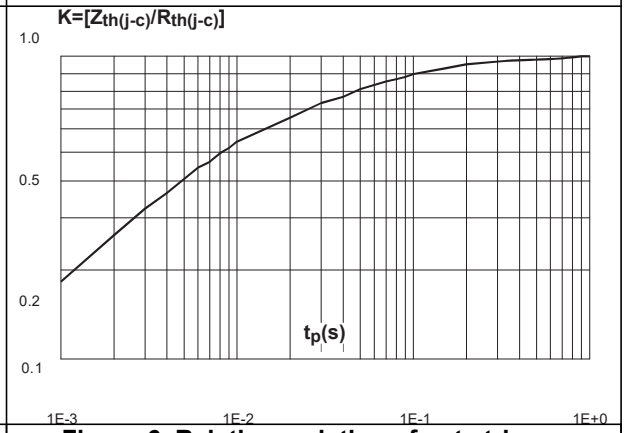


Figure 5. Relative variation of thermal impedance junction to ambient versus pulse duration

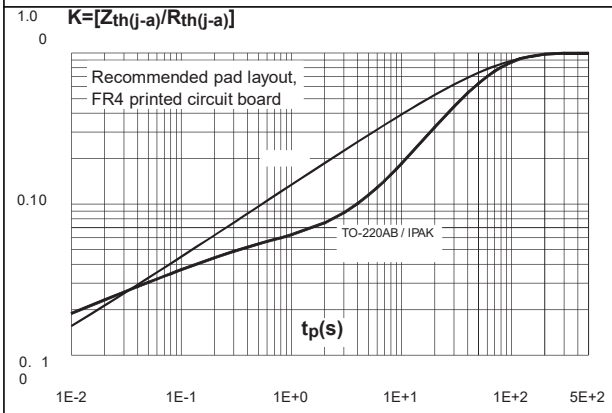


Figure 6. Relative variation of gate trigger current and holding current versus junction temperature

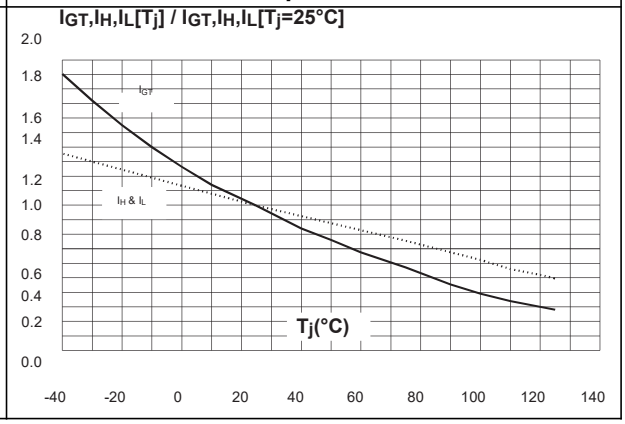


Figure 7. Relative variation of gate trigger and holding current versus junction temperature

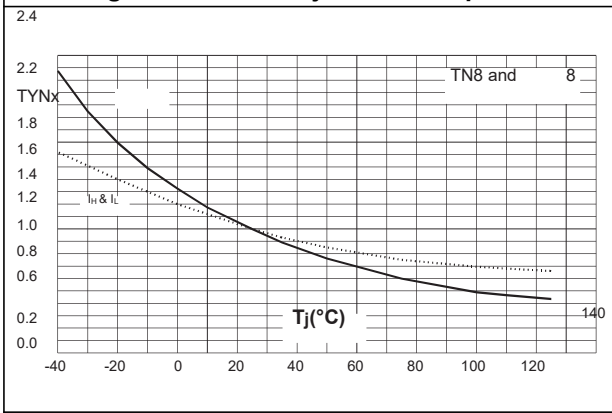


Figure 8. Relative variation of holding current versus gate-cathode resistance (typical values)

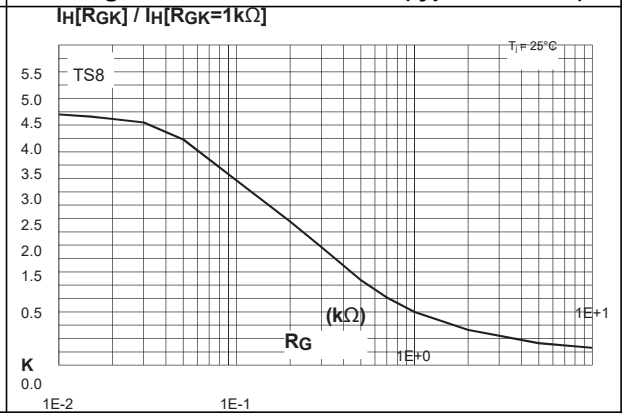


Figure 9. Relative variation of dV/dt immunity versus gate-cathode resistance (typical values)

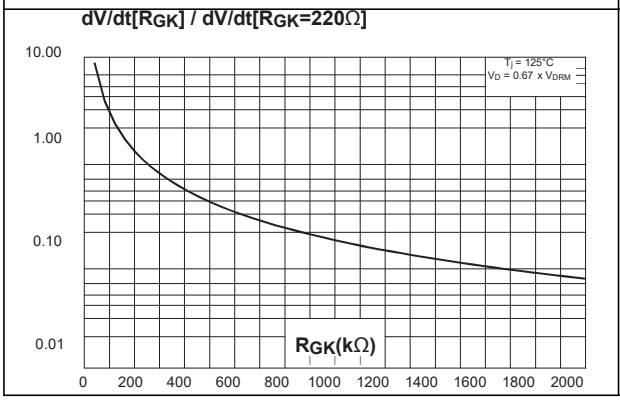


Figure 10. Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values)

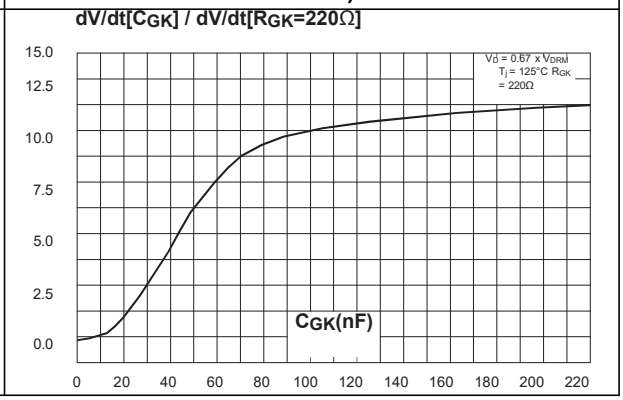


Figure 11. Surge peak on-state current versus number of cycles

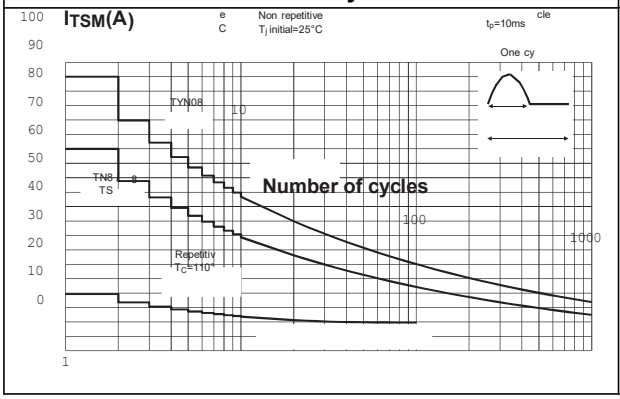


Figure 12. Non-repetitive surge peak on-state current and corresponding values of I^2t

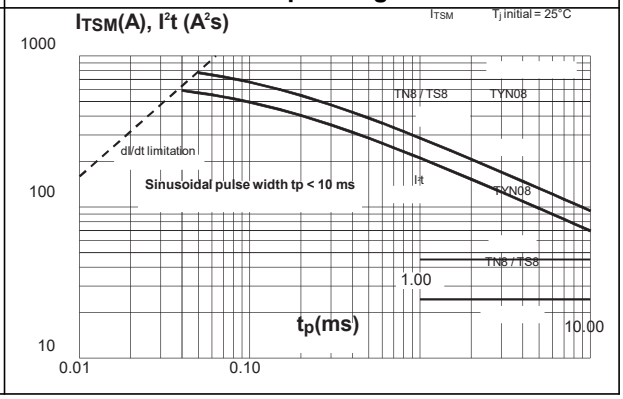


Figure 13. On-state characteristics (maximum values)

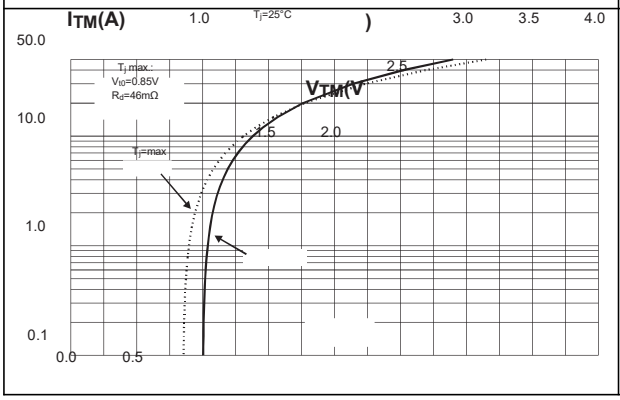


Figure 14. Thermal resistance junction to ambient versus copper surface under tab (DPAK)